Efficiency Enhancement of a Three Phase Hard Switching Inverter Under Light Load Conditions

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***Abstract*—This paper studies the performance of a three phase Hard Switching Inverter (HSI) for low power applications, operating primarily at partial load (7 W, 150 mA-peak, 50 V-peak which is 10 % of its thermally maximum permissible power) in a home appliance application. Analytic methods are used to calculate the losses for different power transistors, resulting in an optimized H-Bridge Inverter (HBI) prototype. The standard hard-switching approach is used, the potential of gate loss reduction by using a Resonant Gate Drive Circuit (RGD) is investigated.**

I. Introduction

DC-AC converters have found a wide range of applications in industry, with very wide power ranges of the loads. The energy conversion efficiency of these converters has become a very important point for many applications. Typically, three types of losses are distinguished between: conduction, switching and gate or control losses [1].

Many researchers have studied HSIs intensively under different loads. In this paper, the type of inverter designed for an extremely light load is investigated and optimized, with a special focus on the very light load application. The efficiency of such an inverter needs to be carefully computed, the different loss types are discussed in detail, expanding the previous work. In [2], the authors evaluated the circuit under small load by employing high voltage IGBTs which are used in mid-power applications under small load conditions of 10 % to 20 % of the inverter's nominal load. In [3], a three phase voltage source micro-inverter topology (with three different topologies of inverters) was studied and tested under low load. MOSFETs were used and the losses were calculated to compare the performances of the different topologies.

This paper studies the performance of a conventionally Pulse Width Modulation (PWM) controlled three phase Hard Switching Inverter (HSI) for an extremely light load (7 W, 150 mA-peak, 50 V-peak). This inverter is designed for a residential appliance. Furthermore, this application has a maximum power point of 70 W, 310 mA-peak, 260 V-peak, which is required only a few times during its lifetime and which is therefore not relevant for its energy consumption. Thus, the inverter is optimized for the very light load operation (10 % of its maximum power). (Any possible output filter is excluded from the study, since, if needed at all, it would depend on the length of the cable used.)

Analytic methods (discussed in Section II) are used to calculate the losses. (500 V - 650 V) MOSFETs and IGBTs are investigated to select the best fit for this application in Section III. Then, the different loss components are compared in detail, their contributions to the total losses are identified, and possibilities to reduce the losses are investigated in Section IV. Test circuit, setup, method and experimental results are discussed in Section V. Finally, conclusions are drawn in Section VI.

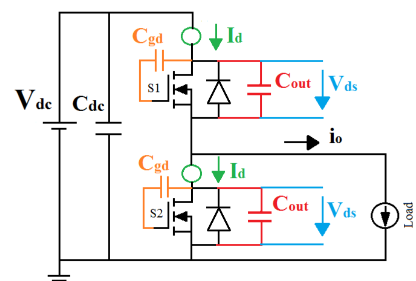

Fig. 1. Single leg of three phase hard switching inverter.

II. HSI Losses Analysis

Figure 1 reviews a single leg of a three phase HSI which contains the DC link capacitor (C_{dc}) and the two power switches (S_1 and S_2) (here: MOSFETs but these can also be replaced by IGBTs with internal or external anti-parallel diodes). Also, it shows the two most relevant parasitic capacitances (C_{gd}, C_{out}).

In this section, the loss components are computed for a single leg, as shown in Figure 1, because the three phase HSI is composed of three identical legs and operated with symmetrical load. As mentioned above, the losses in the HSI are divided into: conduction losses, switching losses and gate drive losses.

In the analysis, the following nomenclature is used, for both types of switches (MOSFET and IGBT):

- R_{on} denotes the on-state resistance for the MOSFETs (R_{dson}) and the differential resistance for the IGBTs (R_{ce}).
- V_{on} denotes V_{ce0}, for IGBTs, and is zero for MOSFETs.
- The forward voltages and differential resistors for diodes are denoted V_{f}, R_{f}, respectively.
- The current drawn by the load is denoted as i_{o}.

Due to the symmetry of i_{o}, the energy losses are calculated for half of the fundamental period and then averaged over half of the fundamental period ($f_{\text{mod}} = 50\,\text{Hz}$).

A. Conduction Losses

The conduction losses (on-state losses) are the losses caused by R_{on}, V_{on} , V_{f}, R_{f} and i_{o}. The energy dissipated in the switch and the diode within one switching cycle (T_{s}) with duty cycle (D_{n}) in switching period number n are given respectively by, [5,10]:

$$E_{\text{condS-n}} = (V_{\text{on}} + R_{\text{on}} i_{\text{o-n}}) i_{\text{o-n}} D_{\text{n}} T_{\text{s}} \quad (1)$$

$$E_{\text{condD-n}} = (V_{\text{f}} + R_{\text{f}} i_{\text{o-n}}) i_{\text{o-n}} (1 - D_{\text{n}}) T_{\text{s}} \quad (2)$$

For such low current, the voltage drop in the channel of the MOSFET is lower than the forward voltage of the body diode of the MOSFET ($R_{\text{on}} i_{\text{o-n}} < V_{\text{f}}$); so the energy lost during the conduction period of the body diode is given by:

$$E_{\text{condD-n}} = (V_{\text{on}} + R_{\text{on}} i_{\text{o-n}}) i_{\text{o-n}} (1 - D_{\text{n}}) T_{\text{s}} \quad (3)$$

The conduction losses are given by (N switching cycles per $0.5 f_{\text{mod}}$) [4]:

$$P_{\text{cond}} = 2 f_{\text{mod}} \sum_{n=1}^{N} (E_{\text{condS-n}} + E_{\text{condD-n}}) \quad (4)$$

B. Switching Losses

1) Switching Losses of the MOSFETs: The switching losses in a power MOSFET depend on its transient behavior, i.e., its turn on (T_{on}) and turn off (T_{off}) times. The times are stated in the data sheet of power MOSFETs for the specific nominal value of load current and voltage, see Table 17 in [12]. If the load changes, these times need to be scaled. So that:

$$T_{\text{on-new}} = t_{\text{ri-new}} + t_{\text{fv-new}} \quad (5)$$

where $t_{\text{ri-new}}$ denotes the scaled current rise time and $t_{\text{fv-new}}$ denotes the scaled voltage fall time at turn on. The general equation for calculating the nominal rise time t_{rn} (at nominal load current) is given by [5,6,7,11]:

$$t_{\text{rn}} = R_{\text{g}} C_{\text{iss}} \ln\left(\frac{V_{\text{dr}} - V_{\text{th}}}{V_{\text{dr}} - V_{\text{gp}}}\right) \quad (6)$$

$$t_{\text{ri-new}} = \frac{t_{\text{rn}}}{I_{\text{n}}} i_{\text{o-n}} \quad (7)$$

where R_{g} is the total (internal plus external) gate resistance, C_{iss} is the input capacitance of one MOSFET, V_{dr} is the driving voltage applied to the gate, V_{th} is the threshold voltage, V_{gp} is the gate plateau voltage (dependence on i_{o} is neglected) and I_{n} is the nominal drain to source current. To calculate $t_{\text{fv-new}}$, the gate current during this time must be calculated [11]:

$$I_{\text{gon}} = \frac{V_{\text{dr}} - V_{\text{gp}}}{R_{\text{g}}} \quad (8)$$

Then, the new voltage fall time at turn on [based on 5]:

$$t_{\text{fv-new}} = \frac{(V_{\text{dc}} - R_{\text{on}} i_{\text{o-n}})}{I_{\text{gon}}} \frac{Q_{\text{gd}}(V_{\text{dc}})}{V_{\text{dc}}} \quad (9)$$

where $Q_{\text{gd}}(V_{\text{dc}})$ denotes the accumulative gate-drain charge, and can be calculated by integrating the gate drain capacitance C_{gd} over V_{dc} [18], where:

$$Q_{\text{gd}}(V_{\text{dc}}) = \int_0^{V_{\text{dc}}} C_{\text{gd}}(v) dv \quad (10)$$

The switching on energy of the upper MOSFET caused by the reverse recovery of the body diode and the output capacitances are given by [4,5]:

$$E_{\text{onrr-n}} = (Q_{\text{rr}} \frac{i_{\text{o-n}}}{I_{\text{n}}} + Q_{\text{out}}(V_{\text{dc}})) V_{\text{dc}} \quad (11)$$

where Q_{rr} is the reverse recovery charge at nominal load current and Q_{out} is the charge of the MOSFET's output capacitance (C_{out}) (one capacitance is charged, while the other one is discharged). This charge can be estimated by integration of the output capacitance over the DC link voltage [18]:

$$Q_{\text{out}}(V_{\text{dc}}) = \int_0^{V_{\text{dc}}} C_{\text{out}}(v) dv \quad (12)$$

The switching on energy during the voltage fall time of the upper MOSFET can be calculated by integrating the power over $t_{\text{fv-new}}$; this is given by:

$$E_{\text{onMv-n}} = \int_0^{t_{\text{fv-new-n}}} v_{\text{ds}}(t) i_{\text{o-n}} dt \quad (13)$$

Also, the switching on energy during the current rise time $t_{\text{ri-new}}$ of the upper MOSFET is given by:

$$E_{\text{onMi-n}} = \frac{1}{2} V_{dc} i_{\text{o-n}} t_{\text{ri-new-n}} \quad (14)$$

The same procedure is followed to calculate the switching losses at turn off of the upper MOSFET:

$$T_{\text{off-new}} = t_{\text{fi-new}} + t_{\text{rv-new}} \quad (15)$$

where $t_{\text{fi-new}}$ denotes the scaled current fall time and $t_{\text{rv-new}}$ denotes the scaled voltage rise time at turn off [5,6,7,11]. Then:

$$t_{\text{fn}} = R_{\text{g}} C_{\text{iss}} \ln \frac{V_{\text{gp}}}{V_{\text{th}}} \quad (16)$$

$$t_{\text{fi-new}} = \frac{t_{\text{fn}}}{I_{\text{n}}} i_{\text{o-n}} \quad (17)$$

The gate current during $t_{\text{rv-new}}$ is given by [11]:

$$I_{\text{goff}} = \frac{V_{\text{gp}}}{R_{\text{g}}} \quad (18)$$

The new voltage rise time at turn off [based on 5]:

$$t_{\text{rv-new}} = \frac{(V_{\text{dc}} - R_{\text{on}} i_{\text{o-n}})}{I_{\text{goff}}} \frac{Q_{\text{gd}}(V_{\text{dc}})}{V_{\text{dc}}} \quad (19)$$

Again, $Q_{\text{gd}}(V_{\text{ds}})$ is found using (**??**).

The switching off energy during the voltage rise time of the upper MOSFET is calculated by integrating the power over $t_{\text{rv-new}}$:

$$E_{\text{offMv-n}} = \int_0^{t_{\text{rv-new-n}}} v_{\text{ds}}(t) i_{\text{o-n}} dt \quad (20)$$

The switching off energy during the current fall time $t_{\text{fi-new}}$ of the upper MOSFET is given by:

$$E_{\text{offMi-n}} = \frac{1}{2} V_{\text{dc}} i_{\text{o-n}} t_{\text{fi-new-n}} \tag{21}$$

Then, the total switching energy for the single leg for switching cycle n is given by:

$$E_{\text{sw-n}} = E_{\text{onrr-n}} + E_{\text{onMv-n}} + E_{\text{offMv-n}} + E_{\text{onMi-n}} + E_{\text{offMi-n}} \tag{22}$$

The switching energy losses are given by (with N switching cycles per $0.5 f_{\text{mod}}$) [4]:

$$P_{\text{sw}} = 2 f_{\text{mod}} \sum_{n=1}^{N} E_{\text{sw-n}} \tag{23}$$

2) Switching Losses of the IGBTs: In this research, the switching losses in the IGBTs are calculated based on [Figures 13, 14 and 16 from [8]], where the figures represent the relationships between the switching losses and collector current, gate resistor and collector emitter voltage, respectively. All these relations show approximately linear dependencies between the IGBT's switching energy and $i_{\text{o-n}}$, R_{g} and V_{dc}. The switching energy for the single leg inverter per one switching cycle is given by [10]:

$$E_{\text{sw-n}} = \frac{E_{\text{n}}(K_{\text{i}} i_{\text{o-n}} + C_{\text{i}})(K_{\text{R}} R_{\text{g}} + C_{\text{R}})(K_{\text{V}} V_{\text{dc}} + C_{\text{V}})}{E_{\text{oi}} E_{\text{or}} E_{\text{ov}}} \tag{24}$$

where:

- K_{i}, K_{R} and K_{V} describe the slope of the E_{ts} line [from the aforementioned Figures 13, 14, and 16] of [8], respectively.
- C_{i}, C_{R} and C_{V} describe the constant values of the E_{ts} line [from the aforementioned Figures 13, 14, and 16] of [8], respectively.
- E_{oi},E_{or},E_{ov} describe energies at nominal load current taken [from the aforementioned Figures 13, 14, and 16] of [8], respectively.
- E_{n} is the total switching losses at nominal load.

Then, the switching losses for the single leg inverter are calculated using (**??**).

C. Gate Losses "Control Losses"

The gate losses are the losses dissipated in the gate resistance (internal plus external) due to the charging/discharging of the input capacitance of the power switch. Thus, the losses during switching cycle n of the two power switches in the single leg of the inverter are given by [5,10] (where, Q_{gt} is the total gate charge at voltage V_{qg} as given in the data sheet):

$$P_{\text{gt}} = 2 Q_{\text{gt}} \frac{V_{\text{dr}}^2}{V_{\text{qg}}} f_{\text{s}} \tag{25}$$

III. Main Circuit Component Selection

The losses occurring in the circuit under the specific load conditions and variable DC link voltages of up to 350 V are computed for 35 members from different families of (500 V - 650 V) CoolMOSs [12], IR-MOSFETs [21], FREDFETs [24] and IGBTs [8] to select the best fitting switch.

Figure 2 shows the computed total losses of a single leg for the best five of the analyzed switches by averaging the losses over one fundamental period. The superior performance of the MOSFETs is evident (blue, green curves) compared to the IGBTs (black curve) over the full range of the DC link voltage. Also, the IR-MOSFETs [21] perform better than the CoolMOSs [12], again, over the full range of the DC link voltage. For experimental verification purposes, the CFD2 family (CoolMOS) (red curve) has been selected [12].

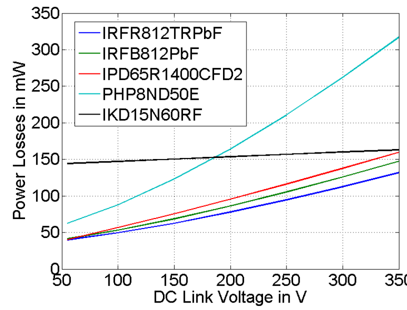

Fig. 2. Single leg computed total losses (conduction, switching and gate) for the best five switches (top to bottom [21,21,12,24,8]).

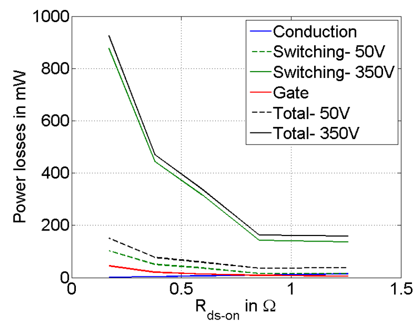

Fig. 3. Single leg computed total losses for CFD2, 50 V and 350 V.

Figure 3 shows how the total losses of a single leg change with the on-state resistance of the CFD2 family. The conduction and gate losses are independent of the DC link voltage. However, the switching losses change with DC link voltage when the switching frequency is constant.

For each MOSFET family, the multiplication of the on-state resistance and input/output capacitances gives a constant value. Increasing the on-state resistance increases the conduction losses (blue curve) and decreases the switching losses (solid and dashed green curves, for 350 V and 50 V, respectively) and gate drive losses (red curves). The solid and dashed black curves show the single leg total losses at a DC link voltage of 350 V and 50 V, respectively.

IV. Efficiency Enhancement

To reduce the overall losses, the contribution of each loss component has been investigated separately as follows:

1) Conduction and Switching Losses: Table I summarizes the computed single leg conduction losses for the selected MOSFET [12] and IGBT [8] (with external diode as stated in the data sheet) at 10 % of the maximum load power for $50\,V \leq V_{dc} \leq 350\,V$. The IGBT has higher conduction losses (at this range of load) compared to the MOSFET because of the additional P region in its structure, which causes an initial voltage V_{ce0}.

Figure 4 shows the computed single leg switching losses, mainly depending on the switch's input and output capacitances. The switching losses of the MOSFET are higher than those of the IGBT in the full DC link voltage range. This is caused by the fact that the output capacitance of the selected MOSFET is higher than the one of the selected IGBT which can be seen in the data sheets ([8] and [12]).

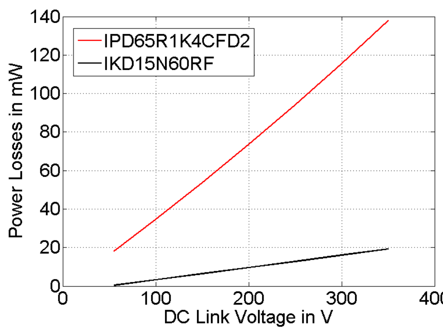

Fig. 4. Single leg computed switching losses selected MOSFET [12]/ IGBT with diode [8] at 10 % of maximum power.

2) Gate Losses and Loss Reduction: The computed gate losses for the single leg inverter are summarized in Table I. This loss component has a considerably high influence on the overall efficiency in the case of applications with high switching frequencies and extremely light load ranges, especially at low DC link voltages. Therefore, a Resonant Gate Driving (RGD) circuit is introduced.

TABLE I
COMPUTED CONDUCTION AND GATE LOSSES, SINGLE LEG.

Switch	Conduction mW losses in mW	Gate mW losses in mW
MOSFET [12]	30.4	6.8
IGBT [8]	89.6	54.3

3) The Resonant Gate Drive (RGD): Many RGD typologies have been introduced and discussed. Most of these works focus on applications with switching frequencies between 500 kHz and 1.5 MHz (e.g., [13]-[17]).

In this paper, the RGD circuit which was proposed in [17] has been employed to reduce the gate losses (Figure 5 (left)). Here again, it is important to select the most suitable switches for the RGD circuit. To select the best fitting switch for the driving circuit, the same procedure as specified in [17] has been followed. In the RGD, the losses are mainly conduction and gate losses, whereby the switching losses are not considered because the RGD is a soft switching topology operating at nearly zero switching losses.

To select the inductor (L_r), the following should be considered: Firstly, it should have low DC internal resistance to reduce the resistive losses in the circuit. Secondly, the current rate in the inductor ($\frac{di}{dt}$) should be lower than the current rate of the selected RGD's MOSFETs to ensure low switching losses. Thirdly, the current capability of the inductor must be higher than the charging/discharging current of the main gate MOSFET ((**??**) and (**??**), respectively).

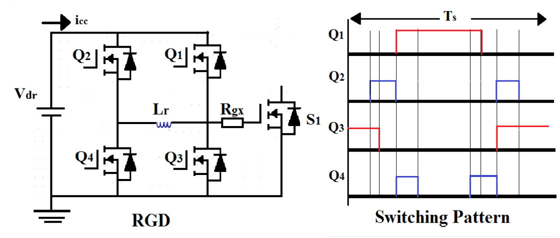

Fig. 5. RGD circuit as proposed in [17] (left), switching pattern (right).

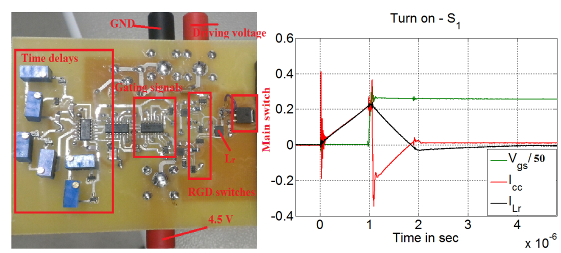

Fig. 6. The RGD prototype (left), measured main MOSFET turn on waveforms (right).

As proposed from the topology, the inductor current should ramp down to zero as soon as Q_2 and Q_4 are turned off. But, as shown in Figure 6 (right), the inductor current (black curve) decreases below zero. This is due to the output capacitance of the selected driving MOSFET of the RGD (the driving MOSFET is Si3588DV [23]). Then, the inductor current approaches zero, while circulating through Q1 and the body diode of Q2. Figure 6 shows the measured gate source voltage of the main switch (green curve and scaled by 1/50), and the red curve shows the recovery energy when the supply current (I_{cc}) becomes negative.

V. DISCUSSION AND RESULTS

A. Test Circuit, Setup and Methods

Figure 7 shows the H-Bridge prototype. Figure 8 (left) shows the test circuit to measure the losses. The circuit was realized from two single legs as an H-Bridge, supplying a large inductor (10 mH) to reduce the ripple current and achieve nearly DC load current. A variable DC-power supply provided the DC link voltage.

The voltage and current input channels of a power analyzer (N5000) [22] were connected to the input and the load of the H-bridge as indicated in Figure 8 (left). As the DC input impedance of the power analyzer voltage channels is in the range of MegOhms, its influence on the power measurement may be neglected, whereas the input capacitances must be considered when comparing the measured losses with those calculated.

Symmetrical Pulse Width Modulation was applied to the circuit to control the load current, where the left leg had a duty cycle of D_{L} and the right leg had a duty cycle of D_{R} as illustrated in Figure 8 (right).

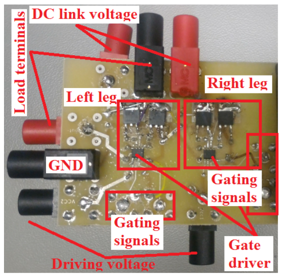

Fig. 7. H-Bridge Prototype.

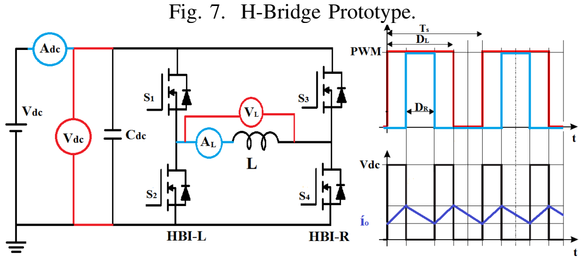

Fig. 8. Test circuit (right), pulse width modulation, load voltage and current (left).

The losses were measured as follows:

- The total losses were measured directly: The sum of switching and conduction losses of the H-Bridge Inverter (two legs) equals the difference of the measured input and output power.
- The switching and conduction losses were separated by taking measurements at two different switching frequencies (different values of the switching frequency multiplier K) and at constant load current. So that:

$$P_{\mathrm{tm}}(Kf_{\mathrm{s}}) = P_{\mathrm{condm}} + K_1 f_{\mathrm{s}}(E_{\mathrm{swm}} + E_{\mathrm{add}}) \quad (26)$$

where P_{tm} are the measured total losses (conduction plus switching), P_{condm} are the measured conduction losses, E_{swm} is the measured switching energy, K is a constant and E_{add} is the energy lost due to the power analyzer channels [22], the load capacitance and the output capacitance of the two switches. The default dead time, introduced by the half bridge driver, successfully prevents cross conduction, but causes forced charging/discharging of the output (and load) capacitances after turning off the previously active channel (under ZVS condition). These additional losses will be reduced by increasing the dead time in the future. The additional charge Q_{add} can be estimated by multiplying the constant capacitances by the DC link voltage and for non-constant output capacitance by integration according to (**??**) for the output capacitance, then:

$$E_{\mathrm{add}} = (Q_{\mathrm{N5000}} + Q_{\mathrm{load}} + Q_{\mathrm{out}}(V_{\mathrm{dc}}))V_{\mathrm{dc}} \quad (27)$$

To calculate the measured switching and additional losses:

$$P_{\mathrm{tm2}} - P_{\mathrm{tm1}} = (K_2 - K_1) f_{\mathrm{s}}(E_{\mathrm{swm}} + E_{\mathrm{add}}) \quad (28)$$

where P_{condm} cancel out each other, the measured switching and additional losses are calculated so that:

$$f_{\mathrm{s}}(E_{\mathrm{swm}} + E_{\mathrm{add}}) = \frac{P_{\mathrm{tm2}} - P_{\mathrm{tm1}}}{K_2 - K_1} \quad (29)$$

- The measured conduction losses can be calculated by:

$$P_{\mathrm{condm}} = P_{\mathrm{tm1}} - K_1 \frac{(P_{\mathrm{tm2}} - P_{\mathrm{tm1}})}{(K_2 - K_1)} \quad (30)$$

- The energy reduction by the use of the RGD is derived as follows: the power consumption of the RGD circuit (Figure 5, R_{gx} was shortened) is compared to the power consumption of the standard gate drive (L_{r} was removed). The power consumption in each case was measured at several switching frequencies. The differences between the readings represent the losses. The difference between the two mean values equals the power saved by the use of the RGD.

B. Measurement Results and Discussion

The MOSFET type ($IPD65R1K4CFD2$) had been selected for a DC load current of $150\,\mathrm{mA}$. (This was the peak value of the sine wave of the load current.) Figure 9 shows the measured and the calculated single leg conduction and switching losses over the range of investigated DC link voltages.

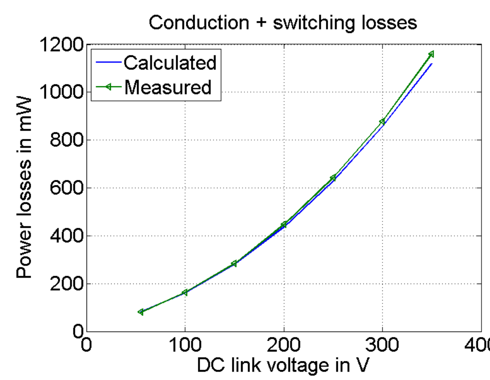

Fig. 9. Measured and calculated total conduction and switching losses, $150\,\mathrm{mA}$ DC load current.

Figure 10 shows the measured and the calculated single leg conduction and switching losses over the range of investigated DC load currents at different DC link voltages.

Finally, the measured gate losses in case of standard hard switching and use of an RGD are compared in Table II, for a single switch. The measured values, in all cases, include losses in the driving MOSFETs. The results show an improvement

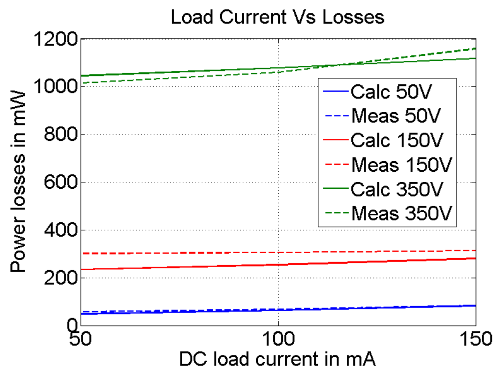

Fig. 10. Measured (dashed curves) and calculated (solid curves) conduction plus switching losses over DC load current at different DC link voltages (50 V, 150 V and 350 V).

in the gate losses when the RGD was used, and the inductor current was 75 mA-peak. However, for higher inductor currents ((**??**) and (**??**)) the RGD consumed more power than the conventional hard switching case. This is explained by the power dissipated in the internal gate resistance at gate current needed to achieve comparable switching speed.

TABLE II
MEASURED FOR SINGLE SWITCH GATE LOSSES AT 20 KHZ

	Stand. hard switching	RGD- 75 mA	RGD- 260 mA
Losses in mW	9.6	6	22.6

VI. CONCLUSIONS

In this paper, the loss performance of a three phase Hard Switching Inverter (HSI) was studied for low power at partial load conditions (7 W, 150 mA-peak and 50 V-peak which is 10 % of its rated power). The loss components were discussed separately in detail.

The measurements were compared with computed total losses based on formulas and parameters from data sheets of the switches. The algorithm was well suited for the optimization procedure and for the selection of the best fit switch under the given operating conditions (DC link voltage (V_{dc}), load current (i_o) and Temperature (T)). The overall computed efficiency at 50 V and 350 V are 98.4 % and 93.6 % respectively; however, taking into account the external load capacitance, the efficiency is reduced to 98 % and 79.7 %, respectively.

Further optimization steps may be carried out, taking advantage of the tested algorithm, e.g., compute the trade-off between the RGD peak current and the overall losses.

Due to the internal gate resistance of the selected MOSFET, together with the peak gate drive current needed to achieve comparable high switching speed, the use of RGD did not reduce the gate drive losses in this application.

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